## REMARKS

Claims 1-14 and 16-30 are pending. The Examiner is maintaining the rejection of claims 1-14 and 16-30 under 35 U.S.C. 102(b) as being unpatentable over Normoyle (5,892,957).

In the previous Office Action Response, the Applicants' representative argued that Normoyle does not teach or suggest any delay introduced by a secondary or slave component. Furthermore, Normoyle does not teach or suggest any delay introduced by a secondary or slave component when responding to a primary component request. For example, Normoyle describes "the randomness of the period of time that the master waits before resending an INT request helps to prevent situations where a given interrupt repeatedly sends interrupts to another device." (column 22, lines 47-50) Normoyle also describes a primary component delaying an interrupt to another primary component. "Hence the delayed retry of the interrupt transaction by the interrupter, especially when it is a processor generating the interrupt to another processor, does not violate any processor memory models." (Summary) Sometimes a master component delays processing of a request from a slave component, but this type of delay is different from the typical Normoyle delay as it is not pseudo random. Plus this delay is still master component delay. "Some such possible constraints relate to delaying the processing of a memory or slave request by a given master until any requests to any other memory or slave, respectively, by that same master are resolved." (Figure 3A Description) Normoyle is not believed to describe any slave or secondary component pseudo randomly delaying a response to a primary component.

In response, the Examiner indicated with reference to Figures 9 and 10 that a primary component issues an interrupt request to a secondary component through a system controller. If the secondary component is unable to receive the interrupt request, the system control issues a negative acknowledgement in response to the request. The master then waits a random period of time and reissues the interrupt request. The Examiner acknowledges that it is the system controller and not the secondary component that issues the negative acknowledgement response, but argues that the negative acknowledgement response is "initiated" by the secondary component because the secondary component can not receive the interrupt request. The Examiner concludes that clearly the delay is determined by the slave device and not by the master device. However, even assuming Examiner's full interpretation, this interpretation does not anticipate specific limitations of the independent claims.

For example, independent claims 1 and 28 explicitly recite "determining a pseudo-random delay prior to responding to the request." Even if we assume the Examiner's argument that the secondary component "initiates" the negative acknowledgement in response to a primary component request, there is no "determining a pseudo-random delay prior to responding to the request." The secondary component does not determine any pseudo-random delay prior to responding to the request. The system controller does not make any such determination prior to responding with a negative acknowledgment to the interrupt request. The primary component does wait a pseudo random period of time before sending another interrupt request, but this is after the system controller or the secondary component responds with a negative acknowledgment to the primary component's request, not "prior to responding to the request."

Furthermore, independent claim 13 recites "a delay mechanism configured to determine values operable to delay responses to requests received through the interconnection module, wherein the values are pseudo-randomly generated values." Independent claim 21 explicitly recites "wherein the plurality of secondary components are configured to determine delay values for adjusting response times to requests received through arbitration logic, wherein the values are pseudo-randomly generated values." Even if we assume the Examiner's argument that the secondary component "initiates" the negative acknowledgement in response to a primary component request, there is no "determining values to delay responses to requests." The pseudo-random delay that Normoyle waits is a primary component waiting before issuing another request. There is no determining values to delay the negative acknowledgement response to an initial request.

Normoyle is believed to describe only primary component pseudo randomly delaying interrupts or non-psuedo randomly delaying responses. The Examiner may attempt to argue that it would be obvious to also apply this to secondary components. The Applicants' representative respectfully disagree. Normoyle pseudo randomly delays primary component interrupts to "prevent situations where a given interrupter repeatedly sends interrupts to another device, preventing the receiving device from sending its own interrupts." (column 22, lines 47-50) The claims are reciting responses to a primary component, so a secondary component would only respond upon receiving a request from a primary component. The motivation for pseudo randomly delaying secondary component responses lies in the ability to test an arbitration logic. For example, it may be useful to test whether arbitration logic fails if a secondary component

waits an excessively long period of time to respond. Nowhere does Normoyle suggest any testing of any arbitration fabric or otherwise.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicant's representative believes that all pending claims are allowable in their present form. If the Examiner has any questions, concerns, or remaining issues for Applicant's representative, the Examiner is encouraged to contact her at the number provided below.

Respectfully submitted,
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